

AMENDMENT TO CLAIMS

1-4. (Canceled)

5. (Previously presented) A semiconductor integrated circuit device comprising:
a silicon substrate;
a plurality of internal circuits each formed on an element region of the silicon substrate;
a first input/output (I/O) cell formed on an I/O cell region of the silicon substrate, the first I/O cell including a first I/O circuit, a first electrode portion horizontally spaced apart from the first I/O circuit with respect to the silicon substrate and a second electrode portion formed on the first I/O circuit, the first electrode portion and the second electrode portion electrically connected to each other and electrically connected to a first internal circuit of the plurality of internal circuits;
a second I/O cell formed on the I/O cell region of the silicon substrate, the second I/O cell including a second I/O circuit and a third electrode portion formed on the second I/O circuit, the third electrode portion electrically connected to a second internal circuit of the plurality of internal circuits; and
an interlayer insulating film formed on the plurality of internal circuits, the first I/O cell and the second I/O cell and exposing the first electrode portion as a probing pad, the second electrode portion as a first terminal pad and the third electrode portion as a second terminal pad.

6. (Previously presented) The semiconductor integrated circuit device according to claim 5, wherein an area of each of the first terminal pad and the second terminal pad is smaller than that of the probing pad.

7. (Previously presented) The semiconductor integrated circuit device according to claim 5, wherein the first internal circuit is a DRAM including a fuse element electrically connected to the probing pad.

8. (Currently amended) A semiconductor integrated circuit device comprising:
a silicon substrate;
a plurality of internal circuits each formed on an element region of the silicon substrate;
a first input/output (I/O) cell formed on an I/O cell region of the silicon substrate, the first I/O cell including a first I/O circuit, a first electrode portion horizontally spaced apart from the first I/O circuit with respect to the silicon substrate and a second electrode portion formed on the first I/O circuit, the first electrode portion and the second electrode portion electrically connected to each other and electrically connected to a first internal circuit of the plurality of internal circuits;
a second I/O cell formed on the I/O cell region of the silicon substrate, the second I/O cell including a second I/O circuit and a third electrode portion formed on the second I/O circuit, the third electrode portion electrically connected to a second internal circuit of the plurality of internal circuits;
an interlayer insulating film formed on the plurality of internal circuits, the first I/O cell and the second I/O cell and exposing the first electrode portion as a probing pad, the second electrode portion as a first terminal pad and the third electrode portion as a second terminal pad;
~~The semiconductor integrated circuit device according to claim 5, further comprising:~~

an insulating protective film formed on a surface of the interlayer insulating film, the insulating protective film covering the probing pad from above with respect to the silicon substrate and exposing the first terminal pad and the second terminal pad;

a first rearrangement wiring formed on a surface of the insulating protective film and electrically connected to ~~either the first terminal pad or the second terminal pad~~; and

a second rearrangement wiring formed on a surface of the insulating protective film and electrically connected to the second terminal pad;

a first solder bump formed on the first rearrangement wiring; and

a second solder bump formed on the second rearrangement wiring.

9. (Currently amended) The semiconductor integrated circuit device according to claim 8, further comprising a first barrier metal layer formed between the first solder bump and a surface of the first rearrangement wiring and a second barrier metal layer formed between the second solder bump and a surface of the second rearrangement wiring.

10. (Currently amended) The semiconductor integrated circuit device according to claim 5, further comprising a plurality of I/O cells each formed on the I/O cell region of the silicon substrate and placed along one side of the silicon substrate, and

wherein each of the plurality of I/O cells ~~is the second I/O cell~~ includes an I/O circuit and an electrode portion formed on a corresponding one of the I/O circuits, the electrode portion electrically connected to a corresponding internal circuit of the plurality of internal circuits.

11-12. (Cancelled)

13. (New) The semiconductor integrated circuit device according to claim 8, further comprising a plurality of I/O cells each formed on the I/O cell region of the silicon substrate and placed along one side of the silicon substrate, and

wherein each of the plurality of I/O cells includes an I/O circuit and an electrode portion formed on a corresponding one of the I/O circuits, the electrode portion electrically connected to a corresponding internal circuit of the plurality of internal circuits.